

### **REMARKS**

Reexamination and reconsideration of this application is respectfully requested in light of the foregoing amendments and the following remarks.

Claims 1-21 are pending in this application. No claims have been amended or canceled. Claims 17-19 and 21 have been withdrawn from consideration due to a restriction requirement.

Applicant notes the Examiner's acknowledgment of Applicant's claim for foreign priority under 35 U.S.C. § 119 and receipt of the certified priority document.

#### **Objection to the Drawings**

Fig. 1 has been objected to in the Office Action. The Examiner has indicated that the figure should be designated as "Prior Art" because it is showing what is illustrated is old. The figure has been amended as suggested in the Office Action. A replacement sheet of the drawing along with an annotated copy of the drawing sheet is submitted with this response. It is respectfully requested that the drawing change be approved and entered.

#### **Rejection Under 35 U.S.C. § 102**

Claims 1-7, 9, 10 and 20 stand rejected under 35 U.S.C. § 102(b) as being unpatentable over Coteus (U.S. Patent No. 6,098,176). Claims 1 and 20 are independent claims. Claim 1 defines a distribution network for distributing a clock signal comprising a sequence of counter signals. The network comprises a plurality of delivery points for facilitating simultaneous detection of different counter signals to provide timing information. The clock signal comprises a modulated carrier, whereby the sequence of counter signals is in the form of an envelope of the carrier.

Coteus describes a clock signal distribution system for providing synchronous clock signals to a plurality of electronic circuit devices. The system includes a clock signal generator for providing a single-frequency sinusoidal clock signal output and a plurality of electronic circuit devices. The network includes interconnected resonant segments of a transmission line connected to the clock signal of the clock signal generator and to the plurality of electronic circuit devices for providing separate synchronous, phase-aligned clock signals to the circuit devices. The transmission line segments have lengths matched to the clock signal frequency wavelengths to eliminate clock signal distribution problems such as skew, jitter and pulse distortions. See the Abstract.

The Office Action asserts that Coteus discloses a clock signal comprising a modulated carrier whereby the sequence of counter signals is in the form of an envelope of the carrier. The Applicant disagrees with this assertion and submits that Coteus does not teach or suggest a modulated carrier whose envelope is used to detect clock counts.

The Office Action refers specifically to the graphs shown in Figs. 2-4 of Coteus. These figures do not provide any disclosure or suggestion of a modulated signal. The clock distribution system of Coteus uses a sinusoidal oscillator that operates at a single frequency (col. 1, lines 33-36). Figs. 2-4 of Coteus show the relative amplitudes of input and output voltages as shown in Fig 1 for different frequencies. Thus, for example, in the arrangement shown in Fig. 2, when the system operates at a frequency of 1 GHz, the input voltage to the transmission line has a normalized amplitude of 1. The output voltage of the transmission line also has a normalized voltage amplitude of 1. Fig. 2 shows how the input and output voltages would vary if the single-frequency source were to be operated at different frequencies. It is submitted that Figs. 2-4 show

transfer functions of the transmission line of Fig. 1, but do not teach modulating a carrier signal in order for an envelope of the modulated signal to provide clock counts.

In addition, claim 1 requires that the plurality of delivery points facilitate simultaneous detection of different counter signals to provide timing information. This feature is not taught in Coteus. Instead, Coteus describes various arrangements in which a clock signal is "divided" between several branches from the source to individual terminating nodes, with each terminating node receiving a portion of the "same" clock signal pulse at the same time. Examples of these dividing configurations are shown in Figs. 5 and 7-12 of Coteus, and in Fig. 1 of the present application, which represents the "Prior Art."

For all of the foregoing reasons, Coteus does not present a *prima facie* case of anticipation for claim 1 and any of the claims dependent on claim 1. It is respectfully requested that the anticipation rejection of claim 1 be reconsidered and withdrawn.

As for claim 20, this claim is directed to a method of distributing a clock signal comprising a sequence of counter signals comprising the steps of (i) providing the clock signal in the form of a modulated carrier, whereby the sequence of counter signals is in the form of an envelope of the carrier, and (ii) simultaneously detecting different counter signals at a plurality of delivery points to provide timing information. For the same reasons as presented with respect to claim 1, Coteus does not disclose or suggest providing a modulated signal as required by the claim. Nor does the reference disclose or suggest simultaneously detecting different counter signals at plurality of delivery points to facilitate to provide timing information as required by claim 20. For all of these reasons, Coteus does not present a *prima facie* case of anticipation for

claim 20. It is respectfully requested that the anticipation rejection of claim 20 be reconsidered and withdrawn.

**Rejections Under 35 U.S.C. § 103**

Claims 8 and 11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Coteus (U.S. Patent No. 6,098,176) in view of Iida et al. (U.S. Patent No. 6,108,465). The arguments presented with respect to the rejection of claim 1, *supra*, are equally applicable to the rejection of claims 8 and 11 and are incorporated herein by reference. Iida et al. do not make up for the deficiencies of Coteus. Iida et al. is directed to an optical pulse generator. It does not disclose or suggest a modulated signal or a plurality of delivery points to facilitate simultaneous detection of different counter signals to provide timing information as required by claim 1. Accordingly, it is requested that the rejection of claims 8 and 11 be reconsidered and withdrawn.

Claims 12-14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Coteus (U.S. Patent No. 6,098,176) in view of Tomiso et al. (U.S. Patent No. 6,737,902). The arguments presented with respect to the rejection of claim 1, *supra*, are equally applicable to the rejection of claims 12-14 and are incorporated herein by reference. Tomiso et al. do not make up for the deficiencies of Coteus. Tomiso et al. is directed to method and system to distribute clock signals in digital circuits. It does not disclose or suggest a modulated signal or a plurality of delivery points facilitate simultaneous detection of different counter signals to provide timing information as required by claim 1. Accordingly, it is requested that the rejection of claims 12-14 be reconsidered and withdrawn.

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For the foregoing reasons, it is submitted that the claims 1-16 and 20 are patentable over the teachings of the prior art relied upon by the Examiner. Accordingly, favorable reconsideration of the claims is requested in light of the preceding amendments and remarks. Allowance of the claims is courteously solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicant's attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due under 37 C.F.R. § 1.17 and due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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